ABSTRACT

A buffer circuit on a first chip coupled between a first circuit on the first chip and a second circuit on a second chip including a driver circuit comprising at least a first PMOS transistor and a second PMOS transistor, one of the source and drain of the second PMOS transistor being coupled to the substrate of the first PMOS transistor, wherein the second PMOS transistor is turned off when a first signal having a voltage level higher than a power supply voltage of the buffer circuit appears at the node, and a gate-tracking circuit coupled to provide a first bias and a second bias to the gate of the first PMOS transistor depending on the signal appearing at the node.